** REMARKS **

Claims 1-11 are pending in this application.

Claims 1-11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Covington, et al.* (USP 4,502,938, hereinafter *"Covington"*) in view of *Gardner, et al.* (USP 6,121,094, hereinafter *"Gardner"*).

With respect to claim 1, the outstanding Action asserts that ***Covington*** teaches a semiconductor substrate (3), a gate oxide (6) on the semiconductor substrate, an ion-selective membrane layer overlaying the gate oxide layer, a source/drain (1, 2) in the semiconductor substrate beside the ion-selective membrane, a metal wire on the source/drain and a sealing layer (11) overlaying the metal wire and exposing the ion-selective membrane layer. Moreover, the outstanding Action asserts that ***Gardner*** teaches a multi-level gate structure including a gate oxide layer (18) with an overlaying tungsten oxide layer (32). The outstanding Action subsequently concludes that one of ordinary skill in the art would modify the teachings of ***Covington*** to include the WO_3 layer overlaying the gate oxide in the gate structure, as taught by ***Gardner***.

Also, in the response to Applicants' arguments, the Examiner asserts that "Gardner teaches that the thickness of the metal oxide layer and the material used for the metal oxide layer are matters of design choice that may vary depending upon specific application requirements or objectives. Therefore, the tungsten oxide layer taught by Gardner can be of an amorphous or crystalline nature, depending on the use". The Examiner also points out that "the test for combining references is what the combination of disclosures taken as a whole would suggest to

one of ordinary skill in the art and that references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures".

The claimed invention, as presently set forth in claim 1, is characterized by an amorphous-Tungsten Oxide (a-WO_3) layer overlying the gate oxide as the sensing membrane of the ISFET. Only amorphous-WO_3 can be used in the ISFET because the resistivity of a-WO_3 is between 10^6 to 10^{10} Ω/cm which is high enough as an insulating film for sensing hydrogen ions without electric leakage in water.

By contrast, ***Covington*** discloses an ISFET structure but fails to teach or suggest any amorphous-Tungsten Oxide overlying the gate oxide layer, and ***Gardner*** teaches a MOS transistor device comprising a metal oxide layer (e.g. tungsten oxide) formed between a gate dielectric layer and a conductor layer but also fails to point out or suggest any amorphous-WO_3.

Additionally, according to the disclosure in column 6, lines 26-34 of ***Gardner***, the metal oxide layer 32, tungsten oxide, is formed by implanting oxygen into the tungsten conductor layer 35 to form the oxygen rich portion 34 and then carrying out a heat treating process to form the metal oxide layer 32 above the gate dielectric layer 18. However, it is well-known that after the heat treating process, e.g. a rapid thermal process or heating in a tube furnace as described in column 6, lines 31-34 of ***Gardner***, the oxygen-rich tungsten layer 34 is not only oxidized as the tungsten oxide layer 32, but also rearranged as a crystalline structure. As such, one of skill in the art would know that the lattice of metal materials will rearrange to crystallize after heat treatment or annealing.

Although ***Gardner*** mentions that "the thickness of the metal oxide layer and the material used for the metal oxide layer are matters of design choice that may vary depending upon specific application requirements or objectives", there is no description of the properties of amorphous WO_3. It is well-known that materials in a MOS gate structure are usually crystallized or polycrystallized. As previously discussed in the Response dated April 10, 2002, neither ***Covington*** nor ***Gardner*** teaches, or remotely suggests, using an amorphous tungsten oxide layer as the sensing membrane of the ISFET. There is simply no motivation for one of ordinary skill in the art to apply an amorphous WO_3 over the gate oxide. Therefore, when one of ordinary skill in the art does combine ***Covington*** and ***Gardner***, such combination would simply yield an ISFET structure with a crystallized WO_3 layer as the sensing membrane which will not work in water for pH measurement because of electric leakage.

Accordingly, even if one of ordinary skill in the art is motivated to combine ***Covington*** and ***Gardner***, such combination does not achieve the present invention as recited in claim 1.

In view of the foregoing, Applicants submit that claim 1 is in proper condition for allowance. Since claims 2-11 are dependent from claim 1, they are also patentable for at least the reasons stated above with respect to claim 1. Additionally, claim 2 requires an ISFET having length, width and a ratio of width/length of the channel of 50μm, 100μm and 20, respectively. However, neither ***Covington*** nor ***Gardner*** teaches or suggests such limitations.

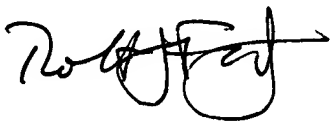
In view of the foregoing, Applicants respectfully request the Examiner for timely allowance of claims 1-11.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2394.

Respectfully submitted,

IPS, Inc.



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